Lecture No 9

Clocking Overhead and Reliable Clocking

Clocking Overhead and Reliable Clocking

- Type of Clocking: The way is data is sampled into storage element
- Register are of two form(Single rank, Dual Rank which is shown in Figure 1)

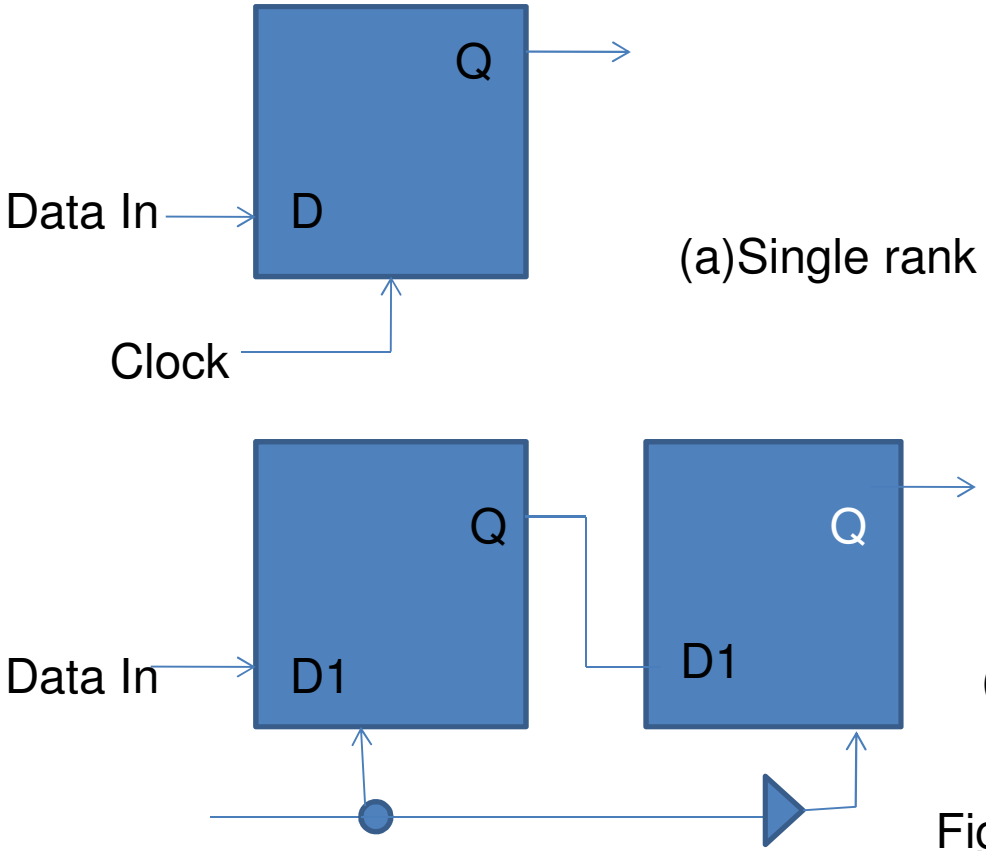

Figure 1. Edge trigger clock

The clocking Overhead

- It is the additional delay in the worst case delay path due to reg. delay & clock. Suppose we define following term.

P_{max}: Max. delay in logic without clock overhead.

P_{min} : Min. delay in shortest logic path

T_w : clock plus width

Δt : Cycle time

t_g: register data setup time

t_d : register output delay after data & clock are enabled

C: clock overhead

$\Delta t = P_{max} + C$

Where $C = t_g + t_w$ (assuming $t_w > t_d$)

Most processor uses transparent clock in fig

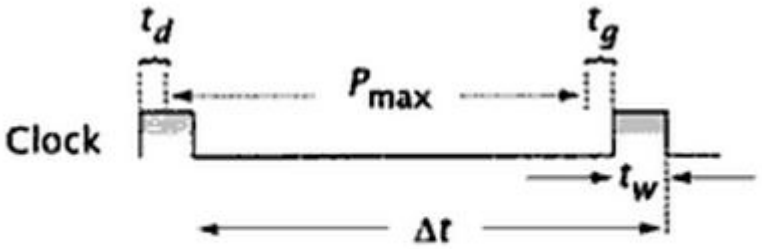

Figure 2.4 Single-rank, transparent clocking.

Pipelined Processors

IF — Instruction fetch from cache into the IR
D — Decode instruction
DF — Data fetch from either memory or register set (ignoring address generation, etc.)
EX — Execute operation

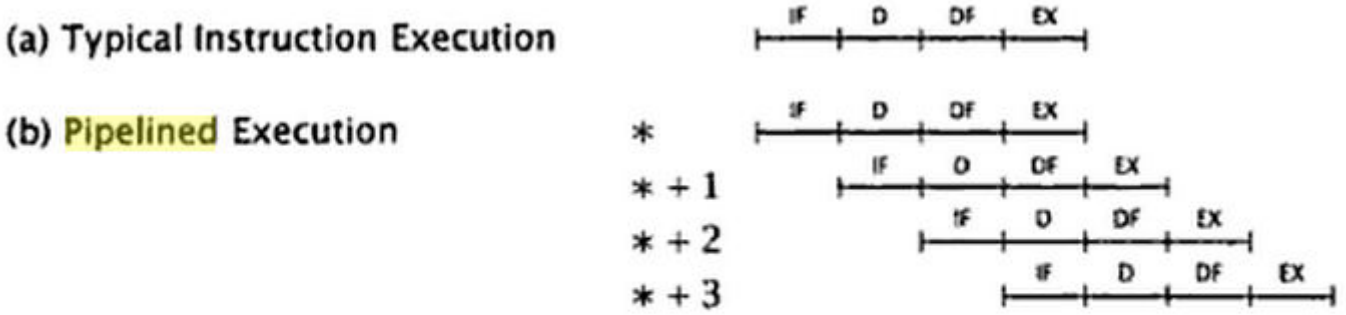

Figure 2.9 Pipelined processors.